

# Grammar Based Modelling and Synthesis of Device Drivers and Bus Interfaces (1998) [\(Make Corrections\)](#) (5 citations)

Mattias O'Nils, Johnny Öberg, Axel Jantsch  
Proceedings of the 24th Euromicro Conference, Vasteras

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**Abstract:** ProGram, a grammar based communication protocol description language, is used for architectural independent modelling of device drivers and bus interfaces for mixed hardware/software systems. The specification of the protocol is separated from the description of processor bus interfaces and operating system device driver interfaces, which ensures a high efficiency in device driver development and maintenance. A synthesis method for device drivers is presented together with results on modelling... [\(Update\)](#)

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...mapped onto the architecture. **Based on extensive research on protocol specification and implementation in hardware and software [8, 9, 10, 11, 12, 13], we will develop a specification method based on a grammar to describe the protocol in an implementation independent way. A...**

... leading group, one of the leading groups in the world and has also published many papers on the topic, see for instance [9, 10, 11, 12, 13, 14, 15, 16, 17, 18]. 7. Scientific and Industrial impact The scientific and industrial impact is greatly increased productivity and...

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HW/SW Communication Protocol Specifications - O'Nils (2001) [\(Correct\)](#)

Architectures, Specification and Synthesis methods for.. - Öberg (2001) [\(Correct\)](#)

Specification and Synthesis of Embedded Datapaths in Communication .. - Öberg (2000) [\(Correct\)](#)

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Mattias O'Nils, Johnny berg, and Axel Jantsch, "Grammar Based Modelling and Synthesis of Device Drivers and Bus Interfaces", Proceedings of the 24th Euromicro Conference, Vasteras, 1998. <http://citeseer.ist.psu.edu/74712.html> [More](#)

```
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264 YACC, Yet another compiler compiler - Johnson - 1975

157 Specification and Design of Embedded Systems (context) - Gajski, Vahid et al. - 1994

19 Synthesis of Concurrent System Interface Modules with Automa.. - Lin, Vercauteren - 1994

18 Grammar-based Hardware Synthesis of Data Communication Proto.. (context) - Oberg, Kumar et al. - 1996

16 A System for Compiling and Debugging Structured Data Process.. (context) - Seawright, Holtmann et al. - 1996

11 Synthesis of the Hardware/Software Interface in Microcontrol.. - Chou, Ortega et al. - 1992

- 7 Comparing Conventional HLS with Grammar -Based Hardware Synt.. - Oberg, Ellerve et al. - 1997
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- 2 High-Level Modeling using Extended Timing Diagrams, A formal.. (context) - Moeschler, Amann et al. - 1992
- 1 Protocol Merging: A VHDL-Based Method for Clock Cycle Minim.. (context) - Ecker, Glesner et al. - 1994
- 1 Writing Device Drivers (context) - Tuggle - 1993

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A Complete Test Strategy Based on Interacting and Hierarchical... - Fummi, Sciuto (Correct)

Description **HDL** code Generation Logic Synthesis **RTL** Description **RTL-HDL** Synthesis **FSMs** Based usually specify, in a hardware description language (**HDL**) by means of a composition of **FSMs**. This paper either from the Statechart description, or from the **VHDL** representation, as explained in Section 2. In the [ipeca4.elet.polimi.it/pub/paper/fs97c.ps.gz](http://ipeca4.elet.polimi.it/pub/paper/fs97c.ps.gz)

Comparing Conventional HLS with Grammar-Based... - Öberg, Peeter... (1997) (Correct)

Hls And 3) Direct Synthesis Of Behavioural **Rtl Vhdl**. 1. Introduction The Goal Of The Case Study designs at behavioural level in languages like **VHDL** and to synthesize detailed circuits automatically. Comparing Conventional HLS with **Grammar-Based** Hardware Synthesis: A Case Study 1 [www.ele.kth.se/ESD/doc/ar97/johnny/norchip97.ps.gz](http://www.ele.kth.se/ESD/doc/ar97/johnny/norchip97.ps.gz)

Automatic VHDL Restructuring for RTL Synthesis... - Corvino, Epicoco... (1998) (Correct)

Automatic **VHDL** Restructuring for **RTL** Synthesis Optimization and Testability Automatic **VHDL** Restructuring for **RTL** Synthesis Optimization and the identification and separation of the two parts (**FSMdata-path**) which can thus be analyzed by using [ipeca4.elet.polimi.it/pub/paper/cei98.ps.gz](http://ipeca4.elet.polimi.it/pub/paper/cei98.ps.gz)

Speeding Up Image Computation by using RTL Information - Meinel, Stangier (2000) (Correct) (1 citation)

Speeding Up Image Computation by using **RTL** Information Christoph Meinel FB Informatik written in an hardware description language (**HDL**) at register transfer level (**RTL**) The term **RTL** is languages that provide **RTL** information like e.g. **VHDL** [8] 2.2 Preliminaries 2.1 Verilog For the [www.informatik.uni-trier.de/~stangier/FMCAD00-submission.ps](http://www.informatik.uni-trier.de/~stangier/FMCAD00-submission.ps)

An approach to Verilog-VHDL interoperability for synchronous... - Borriore Vestman (1997) (Correct) (1 citation)

usually restrict the designer to clock synchronized, **RTL** level, delay free descriptions. Several efforts to re-use a sub-circuit independently of the **HDL** in which it is written. In particular, **VHDL** has Chapman&Hall Publishers 1 An approach to Verilog-**VHDL** interoperability for synchronous designs D. [www.tima-vds.imag.fr/Publications/Charme97.ps](http://www.tima-vds.imag.fr/Publications/Charme97.ps)

Grammatical Evolution: A Steady State approach... - Ryan, O'Neill (1998) (Correct) (1 citation)

production rules are used in a Backus Naur Form (**BNF**) **grammar** definition. Whigham has used **grammars** genome to govern the mapping of a Backus Naur Form **grammar** definition to a program, expressions and [shine.csis.ul.ie/papers/fea98.ps](http://shine.csis.ul.ie/papers/fea98.ps)

Electronic System Design Automation using High Level Petri... - Rokyt, Fengler, Hummel (Correct)

A formal language is used to capture a **RTL** model of the design. The most popular languages References 1. Carlson, S. Introduction To **HDL**-Based Design Using **VHDL**, Synopsys Inc. 1991 2. G. automation tools are used to generate synthesizable **VHDL** code from a Petri net model. For the design of [www.theoinf.tu-ilmenau.de/ra1/ver/hwps98.ps.gz](http://www.theoinf.tu-ilmenau.de/ra1/ver/hwps98.ps.gz)

A Script Environment for the HDL Advisor Evaluation - Gerlach, Hardt, Eikerling... (Correct)

Page 1 of 8 A Script Environment for the **HDL** Advisor Evaluation J. Gerlach, W. Hardt, H.J. Furthermore, an example scenario consisting of four **VHDL** files file1.vhdl file2.vhd Page 2 of 8 [www.uni-paderborn.de/fachbereich/AG/campoag/Papers/GeHaEi96b.ps.gz](http://www.uni-paderborn.de/fachbereich/AG/campoag/Papers/GeHaEi96b.ps.gz)

A Timing-Driven Soft-Macro Resynthesis Method in Interaction... - Conference Dac (Correct)

analysis. The inputs to the design flow is a mixed **RTL** and gate-level **HDL** description in Verilog or **VHDL**, design flow to exploit the interaction between **HDL** synthesis and physical design tasks. During each **RTL** and gate-level **HDL** description in Verilog or **VHDL**, and a timing constraint. The **HDL**-based design [www.cs.nthu.edu.tw/~ylin/publication\\_files/hpsu-dac99.ps](http://www.cs.nthu.edu.tw/~ylin/publication_files/hpsu-dac99.ps)

A Representation for the Binding of RT-Component Functionality... - Roger Ang (1993) (Correct) (1 citation)

the representations for the binding of behavior to **RTL** structure (e.g. CaTa89] Knap89] LGCP91] for the Binding of RT-Component Functionality to **HDL** Behavior Roger P. Ang and Nikil D. Dutt

two outputs. However, in most standard HDLs (e.g. VHDL) the behavioral operation, is a two-input,  
[www.ics.uci.edu/~dutt/pubs/chdl93-repr.ps.gz](http://www.ics.uci.edu/~dutt/pubs/chdl93-repr.ps.gz)

HDL-Based Integration of Formal Methods and CAD... - Borrione... (1996) (Correct) (2 citations)  
 Design Palo Alto, CA, USA, 6-8 November 1996 1 HDL-Based Integration of Formal Methods and CAD Tools  
 circuits. The system currently accepts SMAX[4] and VHDL, and provides equivalence checking, model  
 and synchronized unit delay Finite State Machines (FSM) It is semantically equivalent to a subset of  
[www.tima-vds.imag.fr/Publications/FMCAD-final-diff.ps](http://www.tima-vds.imag.fr/Publications/FMCAD-final-diff.ps)

Efficient Building Block Based RTL Code Generation... - Jens Horstmannshoff... (Correct)  
 Efficient Building Block Based RTL Code Generation from Synchronous Data Flow Graphs  
 Aachen, Germany ABSTRACT This paper presents a RTL-HDL code generation from synchronous data-flow graphs  
 Grotker, and H. Meyr. Digital Receiver Design using VHDL Generation from Data Flow Graphs. In Proc. 32nd  
[www.dac.com/37proceedings/32\\_3.pdf](http://www.dac.com/37proceedings/32_3.pdf)

Formal Verification of the Allocation Step in High Level... - Dushina, Borrione... (Correct)  
 input and produces a VHDL circuit described at the RTL level. The design flow of Amical consists mainly  
 of Implementation of Large Circuits Against HDL Specification. In IEEE Transactions on  
 often written in a hardware description language as VHDL or VERILOG and manipulates the notion of  
[www.tima-vds.imag.fr/Publications//fdl\\_98.ps](http://www.tima-vds.imag.fr/Publications//fdl_98.ps)

Using Prolog and CLP for Designing a Prolog Processor - Illera, al. (1994) (Correct)  
 instruction set into a Register Transfer Level (RTL) code. CLP is used for optimal planning (resource  
 Programming (CLP) The system is developed around VHDL, the industry standard language for hardware  
 to motivate design decisions. Definite Clause Grammars (DCG's) are used to compile (parsing and code  
[mozart.sip.ucm.es/papers/1994/pap94.ps.Z](http://mozart.sip.ucm.es/papers/1994/pap94.ps.Z)

RTL C-Based Methodology for Designing and... - Séméria... (2002) (Correct)  
 4 arjuna@stanfordalumni.org Abstract -A RTL C-based design and verification methodology is  
 on statically scheduled C-based coding style, C to HDL translation, and a novel RTL-C to RTL-Verilog  
[azur.stanford.edu/~lucs/paper/DAC02/09-01-sermeria.ps.gz](http://azur.stanford.edu/~lucs/paper/DAC02/09-01-sermeria.ps.gz)

The VHDL Standard - Meersman (1994) (Correct)  
 International PAR Project Authorization Request RTL Register Transfer Level SCC-20 IEEE Standards  
 .38 5.2.2 Jessi Ac-3 Project: HdI, Component Modelling & Libraries .  
 / Fax: 32(9)220.31.91 email: cme@e2s.be The VHDL Standard An overview of activities, organizations  
[www.vsiwie.tuwien.ac.at/mike/VHDLReport.ps](http://www.vsiwie.tuwien.ac.at/mike/VHDLReport.ps)

VHDL Simulation Acceleration Using Specialized Functions - Taekyoon Ahn (1997) (Correct)  
 compiled code algorithms[3, 4, 5] For highlevel HDLs such as VHDL and Verilog HDL, which are prominent  
 VHDL Simulation Acceleration Using Specialized  
[poppy.snu.ac.kr/papers/ISCAS97\\_ANTA.E.ps](http://poppy.snu.ac.kr/papers/ISCAS97_ANTA.E.ps)

Retargetable Generation of Code Selectors from HDL Processor... - Leupers, Marwedel (1997) (Correct) (14 citations)  
 Retargetable Generation of Code Selectors from HDL Processor Models Rainer Leupers, Peter Marwedel  
 concepts are, however, language independent, and a VHDL frontend is planned. The primitive netlist  
 N S N S N S T (S N S N S N S T (tree grammar processor-specific tree parser base RT template  
[ls12-www.cs.uni-dortmund.de/publications/papers/1997-edtc.ps.gz](http://ls12-www.cs.uni-dortmund.de/publications/papers/1997-edtc.ps.gz)

Standard Verilog-VHDL Interoperability - Victor Berman (Correct)  
 Inc. 1.0 Abstract During the last few years HDLs have become the driver behind the move to top down  
 Standard Verilog-VHDL Interoperability Victor Berman Cadence Design  
[www.vhdl.org/vi/libutil/vhdl\\_verilog/interop.ps](http://www.vhdl.org/vi/libutil/vhdl_verilog/interop.ps)

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A Front-End **VHDL** Editor for Synthesis tools. T. Bouguerba, J.@univ-evry.fr lrg@sophia.inria.fr Keywords: **VHDL grammar**, Framework, Interchange Formats, Multiple CAD  
babar.inria.fr/pub/croap/General/VIUF\_San-Diego.ps[A Concrete Z Grammar - Breuer, Bowen \(1996\) \(Correct\)](#)language Z, following as precisely as possible the **BNF**-like syntax description in the widely used ZA Concrete Z **Grammar** Peter T. Breuer 1 and Jonathan P. Bowen 2

ftp.cs.reading.ac.uk/pub/formal/jpb/zgram.ps

[Implications of VHDL Timing Models on Simulation and... - Krishnaswamy, Gupta.. \(Correct\)](#)and below. At higher levels of abstraction, i.e. **RTL** and above, such timing detail is often unnecessaryThe semantics of delay assignments in event driven **HDL** and logic simulators has been addressed byImplications of **VHDL** Timing Models on Simulation and Software

www.ics.uci.edu/~rgupta/publications/jsa-venkat.ps

[MDG Tools for the Verification of RTL Designs - Anon, Boulerice, Cerny.. \(1996\) \(Correct\)](#)MDG Tools for the Verification of **RTL** Designs K.D. Anon y N. Boulerice y E. Cernytools accept as hardware description a Prolog-style **HDL**, **MDG-HDL**, which allows the use of abstractwe are implementing a translator for a subset of **VHDL** to **MDG-HDL**. Like **ROBDDs**, **MDGs** require a fixed

www.iro.umontreal.ca/labs/lasso/pdb/data/ps\_files/1996/000008.ps.gz

[A Complete Testing Strategy Based on Interacting and... - Fummi, Sciuto \(Correct\)](#)Description **HDL** code Generation Logic Synthesis **RTL** Description **RTL-HDL** Synthesis **FSMs** Based(IFSM)In the standard synthesis approach, the **HDL** description is synthesized and testing analysis isby using Hardware Description Languages (e.g. **VHDL**, Verilog) or graphical tools (e.g. Statemate

ipeca4.elet.polimi.it/pub/paper/fs97d.ps.gz

[VHDL Testability Analysis based on Fault Clustering... - Bietti, Ferrandi.. \(Correct\)](#)of potential testability problems before **RTL** and logic synthesis. Fault injection is performeda useful testability measure must be related to a **HDL** description of a device. We oriented this paper to**VHDL** Testability Analysis based on Fault Clustering and

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[Testable Synthesis of High Complex Control Devices - Fummi Rovati \(1995\) \(Correct\) \(1 citation\)](#)based on interactive **FSMs** (IFSM) extracted from a **HDL** specification (**VHDL** or Verilog)The strategy forbased on hardware description languages (**VHDL** or Verilog) 3]The description of each **FSM** cancontrol devices can be described by interactive **FSMs** (IFSMs) which can be derived from representations

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[Simulation Vector Generation from HDL Descriptions for... - Fallah, Ashar, Devadas \(1999\) \(Correct\) \(20 citations\)](#)Science MIT, Cambridge Abstract Validation of **RTL** circuits remains the primary bottleneck inSimulation Vector Generation from **HDL** Descriptions for Observability-Enhanced Statement**HDL** code or the coverage of all transitions in an **FSM** model of the implementation [1] results in way too

glen.ics.mit.edu/~farzan/papers/occom\_gen.ps

[Analog Hardware Description Languages - Saleh, Rhodes, Christen, Antao \(1994\) \(Correct\) \(1 citation\)](#)And Background Hardware Description Languages (**hdl**s) Have Long Been In Use In The Digital Domain. Thein the digital domain, with standards such as **VHDL** being fairly mature. In this paper we present two

radar-ftp.nrl.navy.mil/pub/MHDL/docs/pubs/AnalogHDL\_gen.ps

[The Use of Hierarchical Information to Test Large Controllers - Fummi Sciuto \(1997\) \(Correct\)](#)directly in a Hardware Description Language (**HDL**)such as **VHDL** or Verilog, or by means ofin a Hardware Description Language (**HDL**)such as **VHDL** or Verilog, or by means of graphical tools that

- rtl hdl vhdl bnf grammar fsm - ResearchIndex document query

STG (SSTG)In Section III the hierarchical **FSM** model (HFSM) is summarized: it allows the  
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Application of a Testing Framework to VHDL... - Bacis, Buonanno... (1997) (Correct) (1 citation)  
flow, from the behavioral specifications, through **RTL** descriptions, down to gate level. In all these  
Application of a Testing Framework to VHDL Descriptions at Different Abstraction Levels  
[15]moreover, analysis of either data-path [7] or **FSM** architectures is usually performed. Our approach  
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Finite State Machines from Feature Grammars - Black (1989) (Correct) (2 citations)  
Finite State Machines from Feature Grammars Alan W Black Centre for Speech Technology  
there does exist a (possibly very large but finite) **FSM**. Thus we could accept a  $n b n$  only where  $n$  is  
There is of course the problem of the size of **FSM** created, as well as the time that is needed to  
www.cstr.ed.ac.uk/publications/publications/1989/Black\_1989\_a.ps

A Synchronous Approach for Hardware Design - Allemand, Bodin, Kountouris, Le .. (1997) (Correct)  
A Synthesis Oriented Implementation (usually As A Rtl Hdl Program) Are Derived. Such Design Methodology  
steps (i.e. refinements, verification, simulation, **HDL** generation, are based on this unique  
description languages (i.e. Verilog [23] or **VHDL** [24]and specific formalisms are used in the  
ftp.irisa.fr/techreports/1997/PI-1131.ps.gz

CSCI 320 Computer Architecture Handbook on Verilog HDL - By Dr Daniel (Correct)  
This is called the Register Transfer Level (**RTL**)Verilog supports all of these levels. However,  
1 CSCI 320 Computer Architecture Handbook on Verilog **HDL** By Dr. Daniel C. Hyde Computer Science Department  
by hardware designers in industry and academia. **VHDL** is the other one. The industry is currently split  
www.ece.umd.edu/class/enee446/verilog-handbook.pdf

Clock Gating on RT-Level VHDL - Schoenmakers, Theeuwes (Correct)  
operation of a tool that performs clock gating on **RTlevel VHDL** by transforming **VHDL** descriptions before  
Clock Gating on RT-Level VHDL Pieter J. Schoenmakers tigger@ics.ele.tue.nl?  
circuit is modeled as a finite state machine (**FSM**)If the **FSM** does not change state, the clock on  
ftp.ics.ele.tue.nl/pub/papers/ls/tigger\_jwis98.ps.gz

BDD-Based Testability Estimation of VHDL Designs - Ferrandi, Fummi, Macii... (1996) (Correct)  
BDD-Based Testability Estimation of VHDL Designs Fabrizio Ferrandi Franco Fummi  
is described in **VHDL** as a network of interacting **FSMDs**. In addition, it is assumed that the testability  
usually specified through a network of interacting **FSMs** (IFSM)In this sense, we can claim that the  
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Model-Based Diagnosis of Hardware Description Languages - Stumptner, WOTAWA (1996) (Correct)  
to programs written at the register transfer level (**RTL**)**RTL** programs represent the last stage of a  
the diagnosis of hardware designs written in the **VHDL** hardware description language. **VHDL** designs are  
www.dbai.tuwien.ac.at/staff/wotawa/cesa96.ps.gz

High Level Synthesis for Designing Custom Computing Hardware - Doncev, Leeser, Tarafdar (1998) (Correct)  
(4 citations)  
In the process, we examined close to 100 different **RTL** designs. The final design had approximately 90,000  
desired system in a Hardware Description Language (**HDL**) and uses logic synthesis tools to produce a  
it on a RIPP10 board, starting from a behavioral **VHDL** description. The total complexity of the design on  
ftp.ece.neu.edu/pub/groups/compeng/ECE-CEG-98-001.ps

A Scalable Hardware Library for the Rapid Prototyping of... - Dörfel, Slomka, Hofmann (1999) (Correct)  
a high-level or a register transfer level (**RTL**) synthesis is carried out for getting optimal  
is the design of communication systems where **C** and **VHDL** are generated from a specification given in **SDL**.  
own controller for each **SDL** finite state machine (**FSM**)In our framework, CADDY-II [3] is used to  
www7.informatik.uni-erlangen.de/RP/paper/rsp299.ps.gz

Speechacts: A Testbed For Continuous Speech Applications - Martin, Kehler (1994) (Correct) (7 citations)  
will concentrate on those. Sphinx accepts a limited **BNF grammar** (no explicit optional elements are  
natural language interpreter SWIFTUS, our Unified **Grammar** (UG) compiler, and the discourse manager.  
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